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May 10, 2004

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Re:	Applicant(s):	Kevin E. Sallese	
	Assignee:	Lattice Semiconductor Corporation	
	Title:	Programmable Logic Device With A Memory-Based Finite State Machine	
	Serial No.:	10/624,965	Filed: 07/21/2003
	Examiner:	Unknown	Group Art Unit: 2183
	Docket No.:	M-15170 US	

Dear Sir:

Transmitted herewith are the following documents in the above-identified application:

(1) Return Receipt Postcard;
(2) This Transmittal Letter (in duplicate); and
(3) Submission of formal drawings with three (3) sheets of formal drawings including Figures 1a, 1b, 2, 3, and 4.

☒ No additional fee is required.
☐ The fee has been calculated as shown below:

CLAIMS AS AMENDED

	Claims Remaining *After* Amendment		Highest No. Previously Paid For		Present Extra		Rate		Additional Fee
Total Claims	20	Minus	20	=	0	x	$18.00	$	0
Independent Claims	3	Minus	3	=	0	x	$86.00	$	0

☐ Fee of _____ for the first filing of one or more multiple dependent claims per application $

☐ Fee for Request for Extension of Time $

Total additional fee for this Amendment: $

☒ Conditional Petition for Extension of Time: If an extension of time is required for timely filing of the enclosed document(s) after all papers filed with this transmittal have been considered, an extension of time is hereby requested.

☐ Please charge our Deposit Account No. 50-2257 in the amount of $

☒ Also, charge any additional fees required and credit any overpayment to our Deposit Account No. 50-2257

Total: $ **0**

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 10, 2004.

Eric Hoover — May 10, 2004 Date of Signature

Respectfully submitted,

Jon W. Hallman
Attorney for Applicants
Reg. No. 42,622

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Kevin E. Sallese		
Assignee:	Lattice Semiconductor Corporation		
Title:	Programmable Logic Device With A Memory-Based Finite State Machine		
Serial No.:	10/624,965	Filing Date:	07/21/2003
Examiner:	Unassigned	Group Art Unit:	2183
Docket No.:	M-15170 US		

Irvine, California
May 10, 2004

Attn: Official Draftsperson
COMMISSIONER FOR PATENTS
Alexandria, VA 22313-1450

SUBMISSION OF FORMAL DRAWINGS

Dear Sir:

Applicants submit three (3) sheets of formal drawings, consisting of Figures 1a, 1b, 2, 3, and 4, in the above-named application. These drawings should replace the formal drawings filed on December 22, 2003. If there are any questions regarding these drawings, please call the undersigned at (949) 752-7040.

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450, on May 10, 2004.

Eric Hoover — May 10, 2004

Respectfully submitted,

Jon W. Hallman
Attorney for Applicants
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